IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940



International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.471 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 15, Issue 11, November 2026

DOI: 10.17148/IJARCCE.2026.1511171

FPGA-Based SVD Accelerator for MRI Image Denoising and Compression

Prof. Geetha B[1], Kunal J Gowda[2], Manoj K R[3], Nithin Gowda H S[4], Nuthan Gowda S R[5]

Assistant Professor, ECE, EAST West Institute of Technology, Bangalore, India[1]

Student, ECE, EAST West Institute of Technology, Bangalore, India[2]

Student, ECE, EAST West Institute of Technology, Bangalore, India[3]

Student, ECE, EAST West Institute of Technology, Bangalore, India[4]

Student, ECE, EAST West Institute of Technology, Bangalore, India[5]

Abstract: The hardware implementation and validation of a Singular Value Decomposition (SVD) accelerator on a Field Programmable Gate Array (FPGA) for efficient Magnetic Resonance Imaging (MRI) image reconstruction and compression. The proposed system employs the One-Sided Jacobi SVD algorithm to decompose image matrices into singular values and corresponding singular vectors, enabling low-rank approximation while preserving significant image information. A 64 × 64 grayscale MRI image is divided into 8 × 8 blocks and processed using the Spartan-7 XC7S50 FPGA on the Arty S7-50 development board Experimental results demonstrate a Peak Signal-to-Noise Ratio (PSNR) of 37.24 dB and Structural Similarity Index (SSIM) of 0.982524 for rank-3 reconstruction, retaining 99.6185% of the image energy.

Keywords: Singular Value Decomposition (SVD), Field Programmable Gate Array (FPGA), MRI Image Processing, One-Sided Jacobi Algorithm, Image Compression, Low-Rank Approximation, Spartan-7, MATLAB.

I. INTRODUCTION

Medical imaging plays a vital role in modern healthcare by providing detailed information about the internal structures of the human body, enabling accurate diagnosis and treatment planning. Magnetic Resonance Imaging (MRI) is one of the most widely used medical imaging techniques because of its ability to generate high-resolution images of soft tissues without exposing patients to ionizing radiation. However, MRI images often contain noise, redundant information, and large amounts of data, which can affect image quality, storage efficiency, and processing performance. Therefore, efficient image processing techniques are essential for improving image reconstruction, compression, and overall computational efficiency.

Singular Value Decomposition (SVD) is a powerful mathematical technique widely used in image processing, data compression, noise reduction, and dimensionality reduction. SVD decomposes a matrix into three components: an orthogonal matrix U, a diagonal matrix Σ containing singular values, and another orthogonal matrix V. By retaining only the most significant singular values, low-rank approximation can be performed to reduce redundant image information while preserving important structural features

II. METHODOLOGY

The supplied system architecture consists of a MATLAB host, UART input and output interfaces, a packet decoder and control finite-state machine, an 8 × 8 input buffer, an SVD processing core, and a response packet builder. The core diagram identifies a sweep controller, rotation engine, column-update logic, norm/sigma generation and floating-point operator IPs for addition, subtraction, multiplication, division and square root. Host-side software reconstructs and validates images from the returned results.

 This work is licensed under a Creative Commons Attribution 4.0 International License

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.471 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 15, Issue 11, November 2026

DOI: 10.17148/IJARCCE.2026.1511171

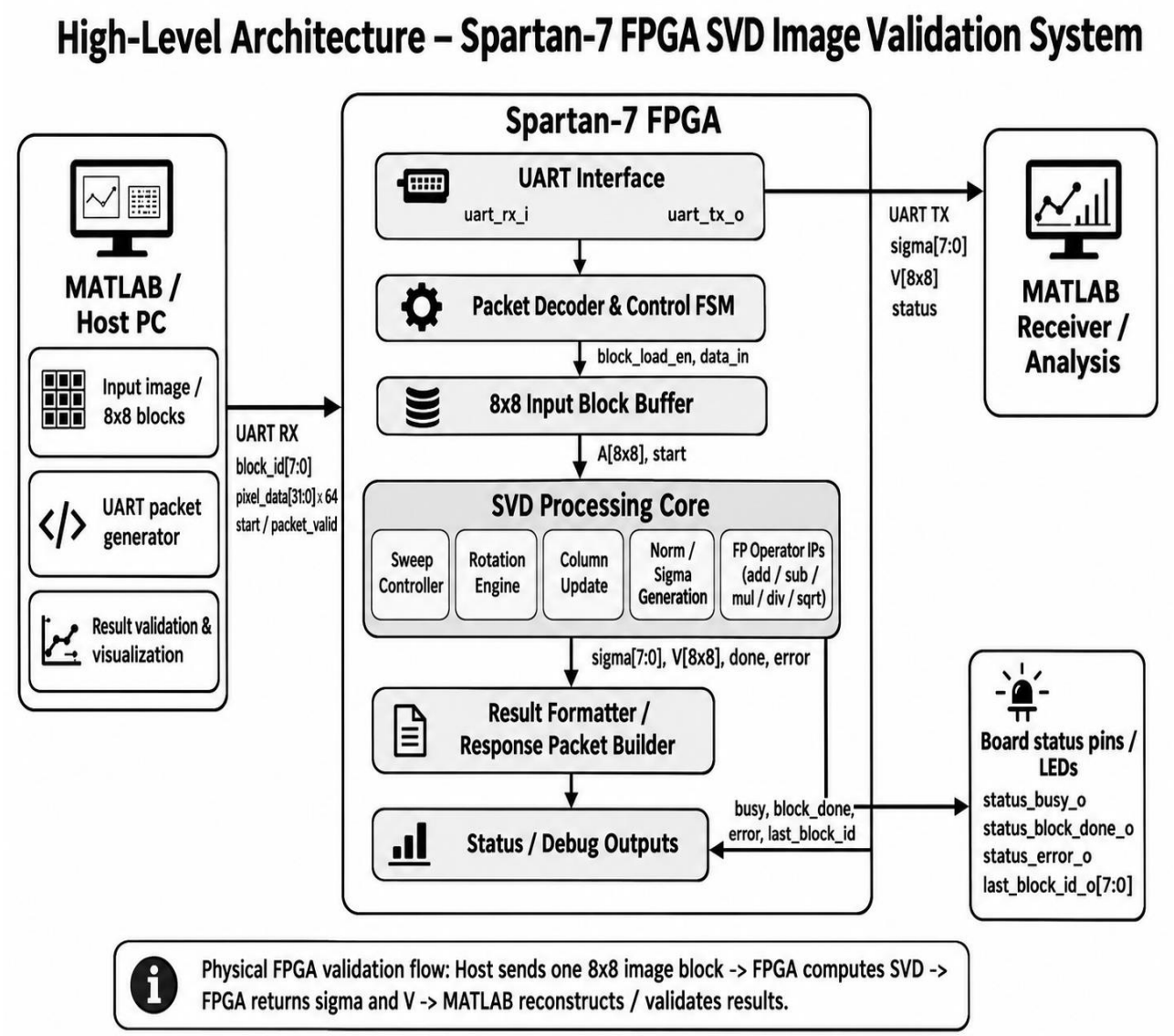


Fig. 1 Block Diagram of High Level Architecture – Spartan-7 SVD Image Validation System

III. RESULT

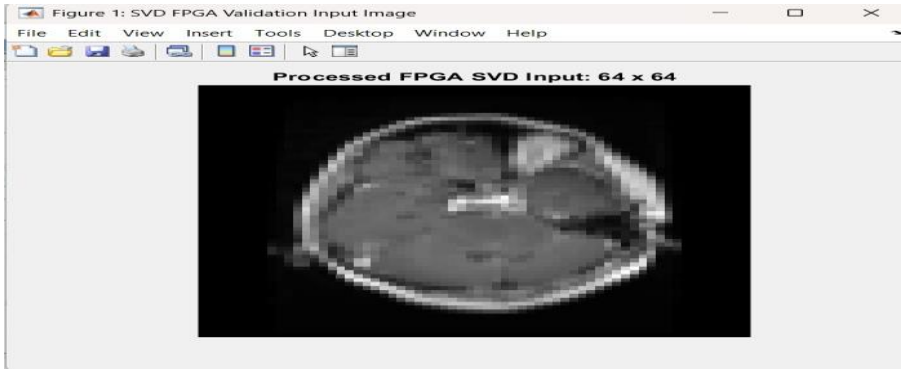


Fig. 2 Processed FPGA SVD Input

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.471 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 15, Issue 11, November 2026

DOI: 10.17148/IJARCCE.2026.1511171

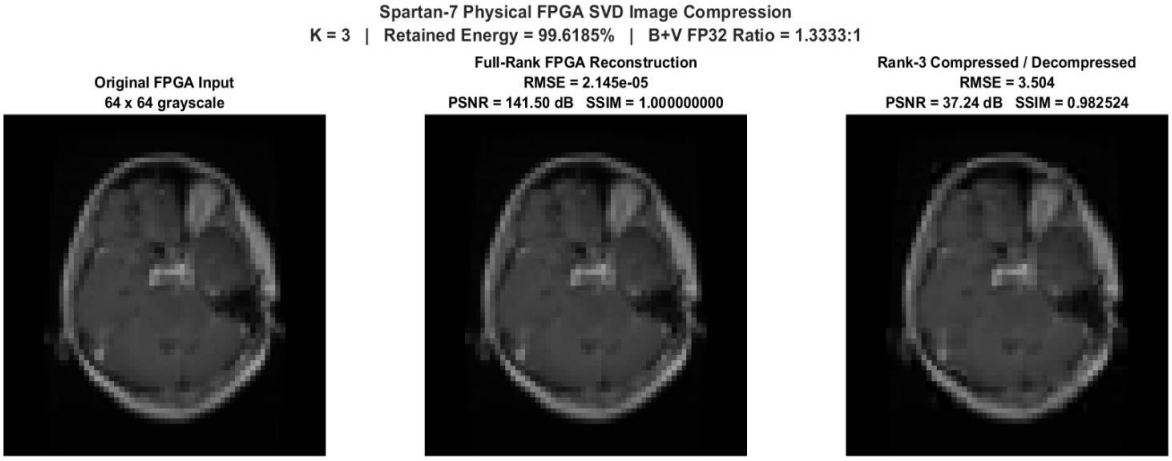


Fig. 3 Original MRI input, full-rank FPGA reconstruction and rank-3 reconstruction

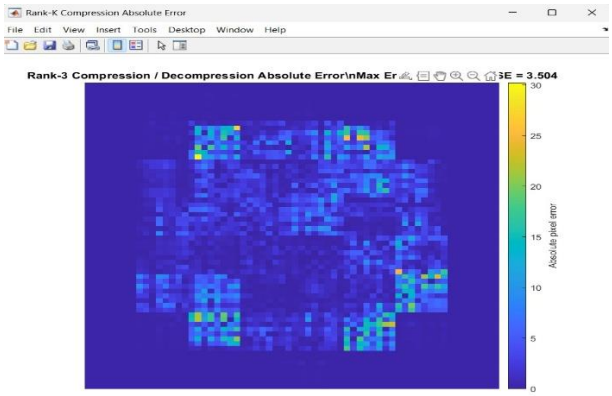


Fig. 4 Absolute pixel-error visualization for rank-3 reconstruction.

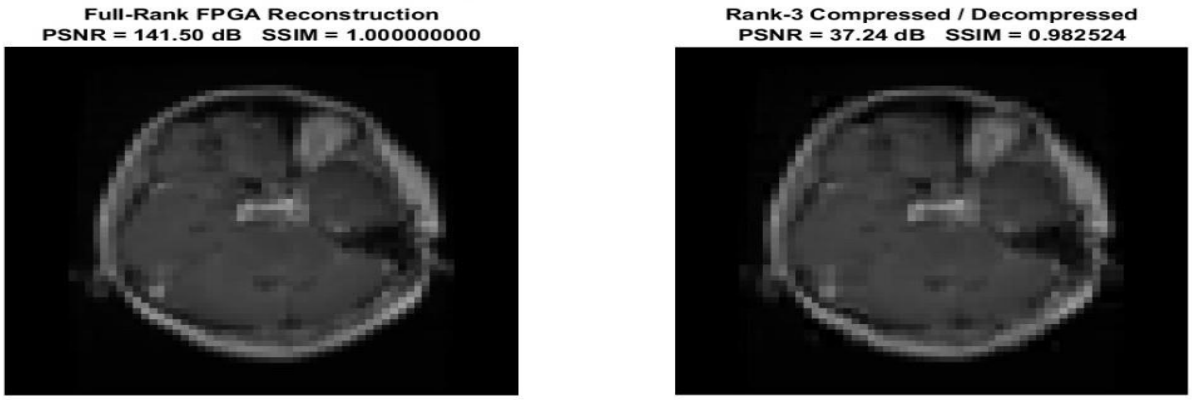


Fig. 5 MRI Image Reconstruction Using SVD with PSNR and SSIM Evaluation

IJARCCE ISSN (O) 2278-1021, ISSN (P) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering

Impact Factor 8.471 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 15, Issue 11, November 2026

DOI: 10.17148/IJARCCE.2026.1511171

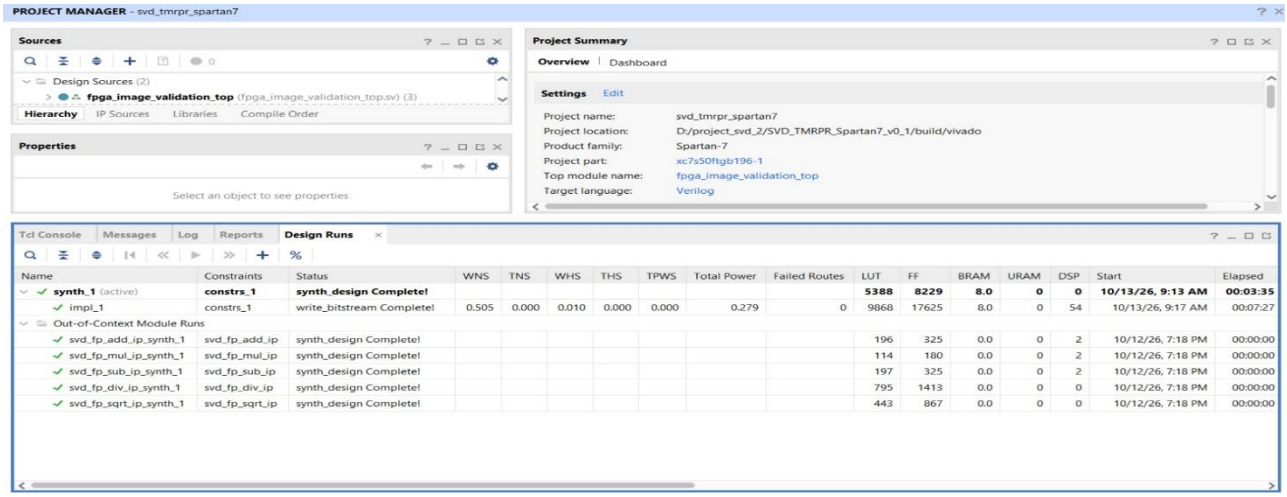


Fig. 6 FPGA Synthesis and Implementation Results in Vivado



Fig. 7 Vivado hardware manager showing the programmed Spartan-7 device

TABLE I PERFORMANCE EVALUATION OF PROPOSED FPGA-BASED SVD RECONSTRUCTION

Performance Parameter	**Full-Rank Reconstruction**	**Rank-3 Reconstruction**
Input Image Size	64x64	64x64
Block Size	8x8	8x8
PSNR(dB)	141.50	37.24
SSIM	1.000000	0.982524
RMSE	2.15×10^{-6}	3.504
Image Energy Retained	100%	99.6185%
Image Quality	Nearly lossless	High similarity
Rank Reduction	No	Yes

IV. CONCLUSION

The project “FPGA-Based SVD Accelerator for Efficient MRI Image Reconstruction and Denoising” successfully demonstrates the hardware implementation of Singular Value Decomposition (SVD) using the One-Sided Jacobi algorithm on the Spartan-7 FPGA (Arty S7-50). The implementation utilizes FPGA-based parallel processing to



International Journal of Advanced Research in Computer and Communication Engineering
Impact Factor 8.471 ⁜ Peer-reviewed & Refereed journal ⁜ Vol. 15, Issue 11, November 2026
DOI: 10.17148/IJARCCE.2026.1511171

accelerate matrix computations, offering a hardware-oriented approach to medical image processing. MATLAB validation and FPGA implementation have been completed, demonstrating the feasibility of the proposed system. By applying SVD-based rank reduction, the project aims to suppress noise, preserve important image features, and support efficient MRI image reconstruction. Overall, the project establishes a foundation for developing high-speed, resource-efficient FPGA accelerators for medical imaging applications, with future potential for real-time processing and improved diagnostic image quality.

V. FUTURE SCOPE

The current evaluation of the proposed FPGA-based SVD accelerator is limited to a single MRI image using rank-3 reconstruction. In future work, the system can be extended to evaluate multiple MRI images with different resolutions, noise levels, and reconstruction ranks to assess its performance and reliability. Comparative analysis with software-based SVD implementations and conventional image denoising techniques can be carried out to determine improvements in computational efficiency and reconstructed image quality.

ACKNOWLEDGMENT

Any achievement, be it scholastic or otherwise does not depend solely on the individual efforts but on the guidance, encouragement and cooperation of intellectuals, elders and friends. A number of personalities, in their own capacities have helped us in carrying out this project work. We would like to take this opportunity to thank them all.

REFERENCES

[1]. L. He and J. Wu, "A High-Performance and Low-Cost FPGA-Based Accelerator for Singular Value Decomposition," in Proc. 2025 6th International Conference on Electrical, Electronic Information and Communication Engineering (EEICE). pp. 923–927, 2025.
[2]. M. M. A. Basiri, "Efficient VLSI Implementations of Singular Value Decomposition," The Journal of Supercomputing, vol. 81, no. 8, 2025.
[3]. L. E. López-López et al., "A Configurable Parallel Architecture for Singular Value Decomposition of Correlation Matrices," Electronics, vol. 14, no. 16, Art. no. 3321, 2025.
[4]. X. Luan, Z. Lin, K. Shi, J. Zhai, and K. Zhao, "Hetero SVD: Efficient SVD Accelerator on Versal ACAP with Algorithm-Hardware Co-Design," in Proc. 62nd ACM/IEEE Design Automation Conference (DAC), 2025.
[5]. "MRI Denoising Using Pixel-Wise Threshold Selection," IEEE Access, vol. 12, pp. 135730–135745, 2024.

 This work is licensed under a Creative Commons Attribution 4.0 International License