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IP-Based RF Power Monitoring Unit

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Abstract: This paper describes the design and development of an interface board for an IP-based RF Power Monitoring Unit (PMU) used with V/UHF and HF radios in shipborne communication systems. The unit accepts up to 16 analog DC voltages, each proportional to the forward or reflected power sensed at a radio. An ADC0816 (8-bit successive-approximation converter with a 16-channel multiplexer) digitizes each channel under the control of an 89V51RD2 (80C51-family) microcontroller. The microcontroller transmits the 16 conversion results over a UART and RS-232 link as a framed packet with start and stop bytes. A PC104 single-board computer encapsulates the data in UDP datagrams and sends it onto an IP network, so that any networked device running the receiver application can display the monitored power. The design was verified by schematic-level simulation in Multisim and by capturing the serial output with a serial terminal tool, and a receiver GUI for eight radios was developed.

Keywords: analog-to-digital conversion, ADC0816, 80C51 microcontroller, power monitoring, RS-232, UDP, embedded systems.

I. INTRODUCTION

Most naval communication is carried over V/UHF and HF radios. Verifying that a transmission has reached its destination by tuning another radio to the same frequency is impractical at scale; a better approach is to monitor the power of every radio centrally. Power monitoring also helps in restricted-area operation, since the frequencies in use can be identified and steps taken to maintain secrecy and avoid conflicts with other bands.

The PMU is one part of an advanced shipborne communication system that provides ship-to-ship, ship-to-shore and ship-to-air communication over MF, HF, VHF and UHF bands, together with intercom. The system's centralized control and monitoring allows remoting of radio equipment and monitoring of radio usage, status and power. The PMU lets any user connected to the network access the forwarded and reflected power of the radio signals.

This work focuses on the interface board of the PMU, which takes the analog power-proportional voltages from the radios, converts them to digital form, sends them serially, and makes them available on an IP network as UDP datagrams. UDP is the connectionless transport protocol defined in RFC 768 [1]. Commercial broadcast power monitors with Ethernet and RS-232 remote interfaces exist, for example the Bird BPME series [10]; the present design addresses the specific 16-channel, serial-to-UDP architecture required here.

Section II presents the system architecture, Section III the hardware, Section IV the firmware and data format, Section V the software tools, Section VI the simulation and test observations, and Section VII the conclusion.

II. SYSTEM ARCHITECTURE

The signal path (Fig. 1) is: V/UHF radio → quartz board → PMU board → serial-to-UDP conversion → Ethernet → PC. The PMU board is the core of the unit and contains the ADC0816, the 89V51RD2 microcontroller, a MAX232 RS-232 transceiver, line drivers and buffers. A power supply unit feeds the whole system (+12 V and +5 V rails are shown in the system diagram).

The PMU board connects to a PC104 single-board computer, which provides the software platform for UDP encapsulation, storage, transmission to the IP network and display. The PC104 is connected to I/O devices (keyboard, mouse, RS-232, VGA display) and to Ethernet through an Ethernet connector. An on/shut-down switch is connected through a connector PCB assembly.

Fig. 1 System block diagrams (original report, p. 4).

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III. HARDWARE DESIGN

A. Analog Front End and ADC

The interface board receives DC voltages proportional to the power transmitted or reflected by each radio, sensed by sensors in the transceiver. Each of the 16 inputs passes through a voltage-dropping trim potentiometer (R1–R16) used for input-level normalization, and a capacitor (C1–C16) provides noise filtering.

The ADC0816 integrates a 16-channel single-ended analog multiplexer with 4-bit latched address inputs, an 8-bit successive-approximation converter and microprocessor-compatible control logic [4], [5]. The converter uses a chopper-stabilized comparator, a 256R voltage divider with analog switch tree and a successive-approximation register (SAR) [4]. A successive-approximation converter comprises a sample-and-hold circuit, a comparator, a SAR and an internal reference DAC. The SAR is initialized with the MSB set; the DAC output (Vref/2) is compared with the sampled input, the bit is cleared if the DAC output exceeds the input, and the binary search continues until all bits have been tested.

The multiplexer output and comparator input are separately accessible, which allows signal conditioning between them. In this design an op-amp amplifies the multiplexed signal to match the dynamic range of the ADC for better signal-to-noise ratio; a DC-DC converter supplies +5 V and −5 V to the op-amp. The amplified signal is fed back to the comparator input, and the resulting 8-bit code is read by the microcontroller. For an assumed 5 V reference, the resolution (one least-significant bit) is

$$V_{LSB} = V_{ref} / 2^8 = 5\ V / 256 \approx 19.5\ mV \quad (1)$$

A conversion begins when the start-conversion (SC) input goes high. The end-of-conversion (EOC) output goes low between 0 and 8 clock pulses after the rising edge of SC, and the result is read by setting output enable (OE) high.

B. Microcontroller

The controller is an 80C51-family 8-bit device (89V51RD2; the parts list gives P89C51RD2HBP in a 64 KB flash, TQFP-44 package) [6], [7]. The report documents the 40-pin DIP pinout and the following features: four 8-bit I/O ports, three 16-bit timer/event counters, a four-priority-level nested interrupt structure, an enhanced UART and an on-chip oscillator. The device is factory-configured for 6 clock periods per machine cycle (“6 clock mode”). A reset requires RST held high for at least two machine cycles while the oscillator is running.

Port usage in the PMU is given in Table I.

TABLE I MICROCONTROLLER PORT USAGE

Port / pin	Function in this design
P0.0–P0.3 (pins 39–36)	ADC multiplexer select lines
P0.4–P0.7	ADC control lines: address latch enable (ALE), start conversion (SC), output enable (OE) and one further control line
Port 1 (output)	Includes the ADC clock output (pin 1, P1.0)
Port 2 (input)	8-bit ADC data
TxD (P3.1, pin 11)	Serial output to the line driver / RS-232 transceiver

Port 0 is an open-drain port; with no external memory it requires external pull-up resistors (10 kΩ), whereas Ports 1–3 have internal pull-ups. The ADC clock is generated by the microcontroller and its frequency can be changed in firmware; the design documentation states a programmed value of 1 kHz.

The serial output is passed to line drivers (AM26LS31) and a MAX232 RS-232 transceiver so that it can be sent to the PC104 over RS-232. Red and green LEDs connected to the AM26LS31 blink during program fusing and data transfer as an indicator.

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C. PC104 Single-Board Computer

The PC104 is designed for on-board systems requiring low power consumption and a wide operating temperature range. It is based on an AMD Geode LX800 CPU running at 500 MHz, with a 16-bit ISA bus and PCI bus, 256 MB DDR SDRAM, two 10/100 Base-T Ethernet ports, two USB ports and four COM ports. Supported operating systems include Windows, MS-DOS, Linux and RTOS-32.

D. Power Conditioning

EMI filters (inductors and capacitors) filter the supply voltage for the board; they pass only positive voltages, so a DC-DC converter generates the negative supply required by some ICs. The principal components are listed in Table II.

TABLE II PRINCIPAL COMPONENTS (FROM THE PROJECT PARTS LIST)

Reference	Component
U1–U7	Op-amp IC 1558
U8	RS-232 transceiver IC (XCVR 232)
U9	AM26LS31/BEA line driver, 16-pin DIP
U10	Analog switch IC 4066B
U11	Microcontroller, 64 KB flash (89V51 / P89C51RD2HBP)
U12	16-channel multiplexer
U13	Quad buffer
U14, U15	EMI filters (SMD)
K1	Reed relay, SPST-NO, 12 V DC
Q1, Q2	Transistors BC107B
CR1	Switching diode 1N5712-1
Y1	Quartz crystal
F3	Time-lag fuse, 0.8 A, 20×5 mm
SW1	Reset switch

IV. FIRMWARE AND DATA FORMAT

The firmware (developed in C51 tools, see Section V) follows the flowchart of the original report:

1. Initialize variables and pins; make Port 2 an input port and Port 1 an output port; start the ADC clock.
2. Set the loop count to 10H (16 channels).
3. Write the channel number to the multiplexer select lines, wait a delay, then set address latch enable high and start conversion.
4. Clear ALE and SC after a delay, then wait 40 ms for end of conversion.
5. Check the EOC pin. If the error branch is taken, “EOC ERROR” is sent and the program jumps to the start; otherwise the output is enabled and, after a delay, the result is read.
6. Store the result in a buffer and increment the buffer address so that data from all 16 channels is collected; decrement the count until it reaches zero.
7. Transmit the 16 bytes serially (routine TX_PKT) and jump to the start.

TX_PKT sends 7Eh through the SBUF register as the start byte, then each of the 16 channel bytes from the data registers byte by byte, then 7Eh as the stop byte. One frame is therefore 18 bytes. Because every channel scan includes a fixed 40 ms wait, a full 16-channel scan takes at least

$$T_{scan} \geq 16 \times 40 \text{ ms} = 640 \text{ ms} \quad (2)$$

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V. SOFTWARE TOOLS

- **Keil µVision/C51:** C compiler, A51 assembler, BL51 linker/locator and OH51 object-to-HEX converter for 80C51 devices.
- **Flash Magic:** Windows software from the Embedded Systems Academy for in-system programming of NXP flash microcontrollers (erase, program, read, blank check, security bits, baud-rate load, boot-loader commands).
- **Docklight V1.9:** RS-232 terminal and monitor used to log and inspect serial data.
- **Multisim (National Instruments):** SPICE-based schematic capture and simulation with microcontroller simulation (MultiMCU).

VI. SIMULATION AND TEST OBSERVATIONS

Schematic simulation. The PMU was captured in Multisim as a top-level schematic (microcontroller model labelled 8052) with two sub-circuits: the ADC section (16 input channels with trim-pot attenuators and RC filters feeding the ADC) and the buffer section (a MAX232E with 1 µF capacitors on a 5 V supply, plus an op-amp stage).

Oscilloscope capture. A Multisim oscilloscope capture of the serial line shows a train of rectangular pulses. The visible settings are a 1 µs/div timebase and 100 mV/div on Channel A; the cursor readout shows 40.249 ms at both T1 and T2 with a level reading of 1.710 V.

Serial capture. The serial output was captured in Docklight V1.9 on COM1 at 19200 baud with no parity (capture timestamp 2/15/2016). The hexadecimal view shows frames delimited by 7Eh bytes, consistent with the packet format of Section IV.

Receiver application. The receiver GUI, "Power Monitoring Unit 1" (software version 1.1), shows eight channels, each with two vertical bar indicators, labelled RADIO:1 to RADIO:8, with Config and Close buttons and a location field.

The report does not include quantitative accuracy, linearity or calibration measurements; these remain to be characterized.

VII. CONCLUSION

A power monitoring unit was designed and developed that monitors the power of V/UHF and HF radios used in on-board communication systems. It accepts 16 analog inputs, digitizes each with the ADC0816 under microcontroller control, and outputs the 16 results serially in a framed packet with start and stop bytes. A PC104 converts the serial data into UDP datagrams for an IP network, so that any device running the receiver application can display the radio powers.

Future work (suggested). Quantitative calibration against a reference power meter; a checksum or sequence field in the packet; and removal of the fixed 40 ms wait by polling EOC.

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